# C8051F00X & C8051F01X DEVELOPMENT KIT USER'S GUIDE

## 1. Kit Contents

The C8051F0xx Development Kit contains the following items:

- C8051F0xx Target Board
- Serial Adapter (RS-232 to Target Board Protocol Converter)
- Silicon Laboratories IDE and Product Information CD-ROM. CD content includes:
    - Silicon Laboratories Integrated Development Environment (IDE)
    - Keil Software 8051 Development Tools (macro assembler, linker, evaluation 'C' compiler)
    - Installation utility (SETUP.EXE)
    - Source code examples and register definition files
    - Documentation
- AC to DC Power Adapter
- RS232 Serial Cable
- 7" Ribbon Cable
- Quick-start Guide
- C8051F0xx Development Kit User's Guide (this document)

# NOTE!

The C8051F0xx device installed on the target board features an internal oscillator which is enabled as the system clock source on reset. After reset, the internal oscillator operates at a frequency of 2.0 MHz by default but may be configured by software to operate at other frequencies (4.0 Mhz, 8.0 MHz or 16 MHz). Therefore, in many applications an external oscillator is not required. However, if you wish to operate the C8051F0xx device at a frequency not available with the internal oscillator, an external crystal may be used. The target board is designed to facilitate the installation of an external crystal at the pads marked Q1. Following are a few part numbers of suitable crystals:

| Freq(MHz) | Digikey P/N | ECS P/N | |
|---|---|---|---|
| 18.432 | X146-ND | ECS-184-20-1 | (20 pF loading capacitance) |
| 11.0592 | X089-ND | ECS-110.5-20-1 | (20 pF loading capacitance) |

Refer to the C8051F0xx datasheet for more information on the configuration of the internal oscillator and the use of external oscillators.

## 2. Hardware Setup

The target board is connected to a PC running the Silicon Laboratories IDE via the Serial Adapter as shown in Figure 1.

1.  Connect one end of the RS232 serial cable to a serial (COM) port on the PC.
2.  Connect the other end of the RS232 serial cable to the DB-9 connector on the Serial Adapter.
3.  Connect the Serial Adapter to the JTAG connector on the target board using the 10-pin ribbon cable.
4.  Connect the AC/DC power adapter to power jack P1 on the target board.
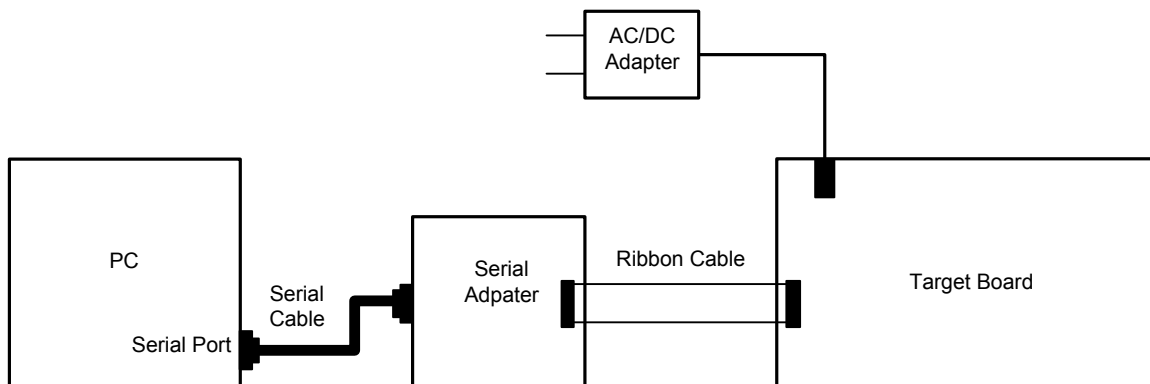
**Figure 1. Hardware Setup**

## 3. Software Setup

The included CD-ROM contains the Silicon Laboratories Integrated Development Environment (IDE), Keil Software 8051 tools and additional documentation.  Insert the CD-ROM into your PC's CD-ROM drive.  An installer will automatically launch allowing you to install the IDE software or read documentation by clicking buttons on the Installation Panel.  (If the installer does not automatically start when you insert the CD-ROM, run "autorun.exe" found in the root directory of the CD-ROM.)    Refer to the "README.TXT" file on the CD-ROM for the latest information regarding IDE known problems and restrictions.

## 4. Integrated Development Environment

The included CD-ROM contains the Silicon Laboratories Integrated Development Environment (IDE).  The Silicon Laboratories IDE integrates a source-code editor, source-level debugger and in-system Flash programmer.  The use of third-party compilers and assemblers is also supported.  This development kit includes the Keil Software A51 macro assembler, linker and evaluation version C51 'C' compiler which can be used from within the Silicon Laboratories IDE.

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## 4.1. System Requirements

The Silicon Laboratories IDE requires:
- Pentium-class host PC running Microsoft Windows 95/98, Windows NT or Windows 2000.
- One available COM port.
- 64 MB RAM and 40 MB free HD space recommended.

## 4.2. Assembler and Linker

A full-version Keil A51 macro assembler and BL51 banking linker are included with the development kit and are installed during IDE installation. The complete assembler and linker reference manual can be found on-line under the *Help* menu in the IDE or in the *"SiLabs\MCU\hlp"* directory (A51.PDF).

## 4.3. Evaluation C51 'C' Compiler

An evaluation version of the Keil C51 'C' compiler is included with the development kit and is installed during IDE installation. The evaluation version of the C51 compiler is the same as the full professional version except code size is limited to 4 kB and the floating point library is not included. The C51 compiler reference manuals can be found in the *"SiLabs\MCU\hlp"* directory (C51.PDF).

## 4.4. Using the Keil Software 8051 Tools with the Silicon Laboratories IDE

To perform source-level debug with the IDE, you must configure the Keil 8051 tools to generate an absolute object file in the OMF-51 format with object extensions and debug records enabled. You may build the OMF-51 absolute object file by calling the Keil 8051 tools at the command line (e.g. batch file or make file) or by using the project manager built into the IDE. The default configuration when using the Silicon Laboratories IDE project manager enables object extension and debug record generation.

To build an absolute object file using the Silicon Laboratories IDE project manager, you must first create a project. A project consists of a set of files, IDE configuration, debug views, and a target build configuration (list of files and tool configurations used as input to the assembler, compiler, and linker when building an output object file).

The following sequence illustrates the steps necessary to manually create a project with one or more source files, build a program and download the program to the target in preparation for debugging. (The IDE will automatically create a single-file project using the currently open and active source file if you select **Build or Make Project** before a project is defined.)  Refer to **Applications Note AN104** in the "Documentation" directory on the CD-ROM for additional information on using the Keil 8051 tools with the Silicon Laboratories IDE.

### 4.4.1.  Creating a New Project

1.  Select **File -> New File** to open an editor window. Create your source file(s) and save the file(s). (Color syntax highlighting will be enabled once the file is saved with a recognized extension such as .c, .h or .asm.)
2.  Right-click on "New Project" in the **Project Window**. Select **Add files to project**. Select a file to add to the project in the file browser and click Open.
3.  Select the **File Group** to which you want to add the file(s) and click **Add Group**. Repeat steps 2 and 3 for each file you want to add to the project.
4.  For each of the files in the **Project Window** that you want assembled, compiled and linked into the target build, right-click on the file name and select **Add file to build**. Each file will be assembled or compiled as appropriate (based on file extension) and linked into the build of the absolute object file.

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### 4.4.2. Building and Downloading the Program for Debugging

1.  Once all source files have been added to the target build, click on the **Build** button in the toolbar (or select **Project -> Build/Make Project** to build and download the program to the target hardware for debug.

    By default, if the program build is successful, the IDE will automatically connect to the target and download the program for debug.  (This may be disabled by deselecting **Enable automatic connect/download after build** in the **Projects -> Target Build Configuration** dialog.)  If errors occur during the build process, the IDE will not attempt the download.

2.  Save the project when finished with the debug session to preserve the current target build configuration, editor settings and the location of all open debug views.  To save the project, right-click on the **New Project** entry in the **Project Window** and select **Save as a project**.

## 4.5. Example Source Code

Example source code is provided in the "Examples" directory on the Silicon Laboratories IDE CD-ROM.  These files may be used as a template for code development.  By default, the C8051F0xx exits reset with the watchdog timer (WDT) enabled.  The BLINK.ASM file used in the "Quick Start" demo illustrates the correct method for disabling the WDT as well as configuring the Port I/O crossbar.

## 4.6. Register Definition File

Register definition files defining all SFR registers and bit-addressable control/status bits, are provided in the "Examples" directory on the Silicon Laboratories IDE CD-ROM.  The register and bit names used in this file are identical to those used in the C8051FxxX datasheets.  These files are also installed in the default search path used by the Keil Software 8051 tools.  Therefore, when using the Keil 8051 tools (A51, C51) it is not necessary to copy a register definition file to each project's file directory.
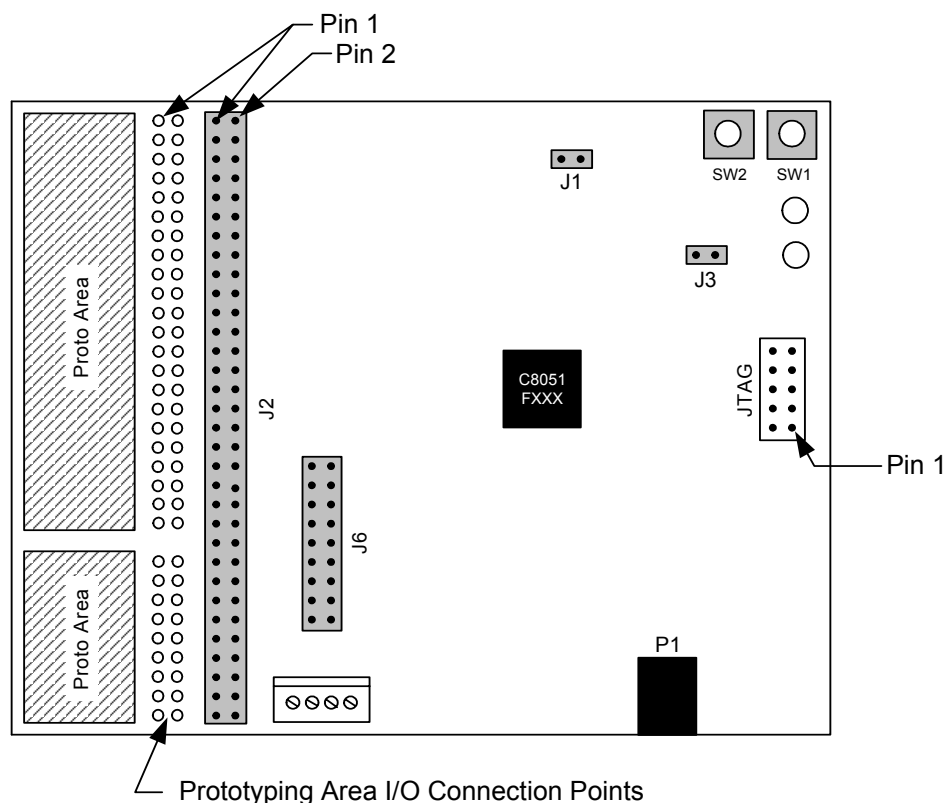
# 5. Target Board

The target board provides access to all C8051F0xx signals (except the four JTAG signals: TCK, TMS, TDO and TDI used to connect the Serial Adapter) via the 64-pin connector J2.  A small through-hole prototyping area is also provided.  All I/O signals routed to connector J2 are also routed to through-hole connection points between J2 and the prototyping area (see Figure 2).  The signal layout pattern of these connection points is identical to the adjacent J2 connector pins.  Table 1 shows the pin-out of the J2 connector.

An Analog I/O Configuration Jumper (J6) provides the ability to route analog I/O signals from the C8051F0xx to a terminal block in addition to connector J2 by installing two shorting blocks on J6.  It also allows the DAC outputs to be connected to Comparator 0 inputs or to two ADC inputs.  Refer to Figure 3 to determine the shorting block installation positions required to connect the desired analog signal to the terminal block.

Two switches and two LEDs are provided on the target board.  Switch SW1 is connected to the RESET pin of the C8051F0xx.  Pressing SW1 puts the C8051F0xx in its hardware-reset state.  The C8051F0xx will leave the reset state after SW1 is released.  Switch SW2 is connected to the C8051F0xx's Port 1.7 (P1.7) general purpose I/O (GPIO) pin.   Pressing SW2 generates a logic high signal on the P1.7 pin.  Releasing SW2 returns the signal level to logic low.  The P1.7 signal is also routed to a pin on the J2 connector.  Remove the shorting block from J1 to disconnect SW2 from P1.7.

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The LED labeled PWR is used to indicate a power connection to the target board. The LED labeled P1.6 is connected to the C8051F0xx's Port 1.6 (P1.6) GPIO pin through jumper J3. The P1.6 signal is also routed to a pin on the J2 connector. Remove the shorting block from J3 to disconnect the LED from P1.6.



**Figure 2. C8051F0xx Target Board**

## 5.1. C8051F0xx Target Board Connectors

Refer to Figure 2 for the locations of the following connectors:

P1      - Power connector (accepts input from 7 to 15 VDC unregulated power adapter)
J1      - Connects SW2 to C8051F0xx Port 1.7 pin
J2      - 64-pin I/O connector providing access to all C8051F0xx I/O signals
J3      - Connects LED D3 to C8051F0xx Port 1.6 pin
JTAG   - Used to connect the Serial Adapter to the target board via a 10-pin ribbon cable

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## 5.1.1. C8051F0xx Target Board I/O Connector Pin Descriptions (J2)

| Pin | Description | | Pin | Description |
|-----|-------------|---|-----|-------------|
| 1 | +VD (digital voltage supply) | | 28 | P3.7 |
| 2 | XTAL1 | | 29 | P3.4 |
| 3 | P1.6 | | 30 | P3.5 |
| 4 | P1.7 | | 31 | P3.2 |
| 5 | P1.4 | | 32 | P3.3 |
| 6 | P1.5 | | 33 | P3.0 |
| 7 | P1.2 | | 34 | P3.1 |
| 8 | P1.3 | | 36 | /RST |
| 9 | P1.0 | | 39,41,42 | GND (digital ground) |
| 10 | P1.1 | | 45,47,63 | GNDA (analog ground) |
| 11 | P0.6 | | 46,64 | +VA (analog voltage supply) |
| 12 | P0.7 | | 48 | DAC0 |
| 13 | P0.4 | | 49 | CP1- |
| 14 | P0.5 | | 50 | DAC1 |
| 15 | P0.2 | | 51 | CP1+ |
| 16 | P0.3 | | 52 | CP0- |
| 17 | P0.0 | | 53 | VREF |
| 18 | P0.1 | | 54 | CP0+ |
| 19 | P2.6 | | 55 | AIN0 |
| 20 | P2.7 | | 56 | AIN1 |
| 21 | P2.4 | | 57 | AIN2 |
| 22 | P2.5 | | 58 | AIN3 |
| 23 | P2.2 | | 59 | AIN4 |
| 24 | P2.3 | | 60 | AIN5 |
| 25 | P2.0 | | 61 | AIN6 |
| 26 | P2.1 | | 62 | AIN7 |
| 27 | P3.6 | | | |

**Table 1. J2 Pin Descriptions**

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## 5.1.2. C8051F0xx Target Board Analog I/O Configuration Jumper (J6)

Analog signals may be routed to the AIO 0 and AI01 posts of the terminal block by installing a shorting jumper between two adjacent pins on J6.
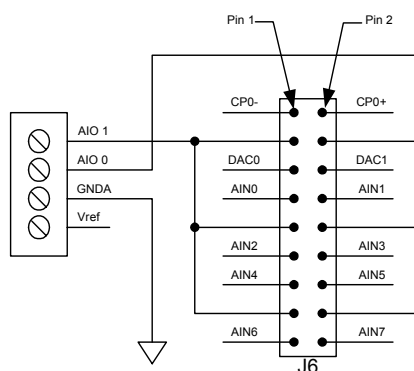


**Figure 3. J6 Configuration Jumper**

## 5.1.3. C8051F0xx Target Board JTAG Connector Pin Description

| Pin | Description |
|---|---|
| 1 | 2.7 to 3.6 VDC Input |
| 2, 3, 9 | Ground |
| 4 | TCK |
| 5 | TMS |
| 6 | TDO |
| 7 | TDI |
| 8, 10 | Not Connected |

**Table 2. JTAG Connector Pin Descriptions**

## 6. Serial Adapter

The Serial Adapter provides the interface between the PC's RS232 serial port and the C8051F0xx's JTAG-based, in-system debug/programming circuitry. The Serial Adapter may be powered from the target board via the Serial Adapter's 10-pin JTAG connector or it may be powered directly from the included AC/DC power adapter. (The target board can not be powered from the Serial Adapter.)

Notes:
1. When powering the Serial Adapter via the JTAG connector, the input voltage to the JTAG connector's power pin must be 3.0 to 3.6 VDC. Otherwise, the Serial Adapter must be powered directly by connecting the AC/DC adapter to the Serial Adapter's DC power jack.
2. The Serial Adapter requires a target system clock of 32 Khz or greater.

| Pin | Description |
|---|---|
| 1 | 3.0 to 3.6 VDC Input |
| 2 | Ground |
| 4 | TCK |
| 5 | TMS |
| 6 | TDO |
| 7 | TDI |
| 3,8,9,10 | Not Connected |

**Table 3. JTAG/DEBUG Connector Pin Descriptions**
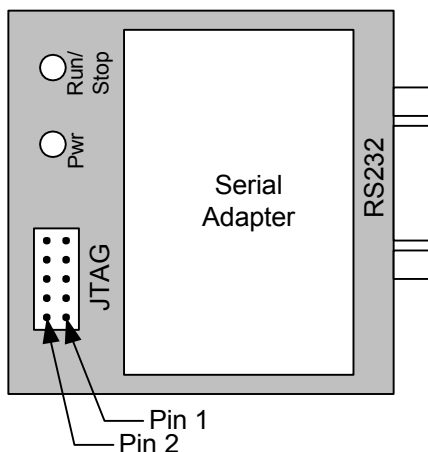


**Figure 4. Serial Adapter JTAG/DEBUG Connector**

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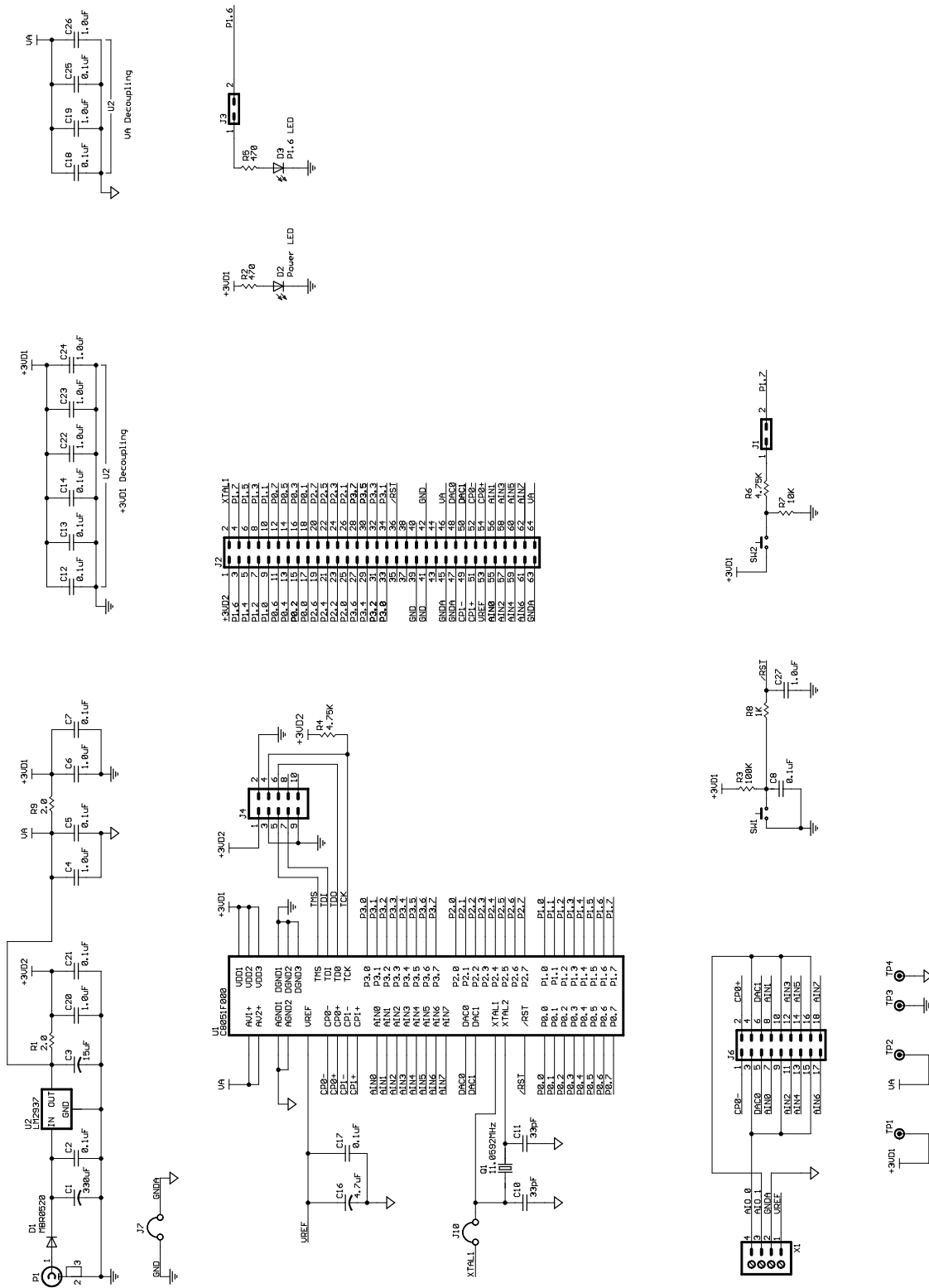
## 7. Schematic



**Figure 5. C8051F0xx Target Board Schematic**

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